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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/579,542	05/26/2000	Cheng Chung Lin	TSMC2000-079	7369

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EXAMINER
VINH, LAN

ART UNIT	PAPER NUMBER
1765	10

DATE MAILED: 08/19/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

MK-10

Office Action Summary	Application No. 09/579,542	Applicant(s) LIN ET AL.	
	Examiner Lan Vinh	Art Unit 1765	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 July 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-3, 7, 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Huang (US 6,252,303) in view of Murugesh et al (US 6,228,781)

Huang discloses a method for depositing a low k dielectric constant layer as inter-layer dielectric. This method comprises the steps of:

depositing a layer of low k fluorosilicate glass (FSG)/low dielectric constant material by HDP/ plasma enhanced chemical vapor deposition (PECVD) (col 1, lines 14-15; col 2, lines 51-52) using a very low bias power (col 3, lines 15-16) reads on depositing a first layer of low dielectric constant material by PECVD at a first power level

then depositing a layer of low k fluorosilicate glass (FSG)/low dielectric constant material by HDP/ plasma enhanced chemical vapor deposition (PECVD) (col 1, lines 14-15; col 2, lines 51-52) using high bias power (col 3, lines 16-19) reads on depositing a second layer of low dielectric constant material by PECVD at second power level that is higher than the first power level

Unlike the instant claimed invention as per claim 1, Huang does not explicitly disclose repeating the steps of depositing the FSG/low dielectric constant material at

low and higher power level to reach a thickness of the FSG/low dielectric constant material layer.

However, Murugesh discloses a method for depositing FSG (low k material) layer comprises the step of continuously depositing FSG layer at different power level (low and high) in a cycle until the FSG layers reach a desired thickness (col 13, lines 36-38). Murugesh' s teaching reads on repeating the steps of depositing the low dielectric constant material at low and higher power level to reach a thickness.

Hence, one skilled in the art would have found it obvious to modify Huang's method by adding the step of depositing the low dielectric constant material layer at low and higher power level until reaching a desired thickness as per Murugesh because Murugesh teaches that the cycle of deposition until the FSG layer having a desired thickness resulting in a film/layer having a low dielectric constant which has a good gap filling characteristic and stability (col 13, lines 38-40)

Regarding claim 2, Huang discloses that low k dielectric films/layer includes fluorinated silicate glass (FSG)

Regarding claim 3, Huang discloses forming the first FSG layer having a thickness of 0.8-1.0 microns (1000 angstroms) (col 3, lines 11-12) reads on the claimed range of 700-1000 angstroms

Regarding claim 7, Huang discloses using the low bias power of less than 100 W (col 5, lines 16-17) overlaps the claimed range of between 70-200 W

Regarding claim 8, since it is known in the art that oxide /low dielectric constant material has a flat band voltage of –1.82 V exhibiting a low leakage current density (see

prior art of record for evidence of this basis), it would have been obvious to one skilled in the art to employ a low dielectric constant material having a flat band voltage that is less than about –3 V to achieve lower leakage current density.

3. Claims 4-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Huang (US 6,252,303) in view of Murugesh et al (US 6,228,781) and further in view of Gardner et al (US 6,140,688)

Huang method as modified by Murugesh has been described above in paragraph 2. Unlike the instant claimed inventions as per claims 4-5, Huang and Murugesh do not specifically disclose the claimed thickness of the low dielectric material layer.

However, Gardner in a method of depositing multi-layer dielectric layers, teaches that thickness of dielectric layer is a variable, if desired the thickness is modified to achieve a certain performance level (col 3, lines 4-6)

Since Huang discloses that other thickness of the FSG layer is possible (col 3, lines 12-13), one skilled in the art would have found it obvious to vary the FSG layer thickness of Huang and Murugesh in view of Garner teaching by conducting routine experimentation to achieve specific thickness of FSG layer for the purpose of obtaining the best deposition rate.

4. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Huang (US 6,252,303) in view of Murugesh et al (US 6,228,781) and further in view of Cheung et al (US 6,287,990)

Huang method as modified by Murugesh has been described above in paragraph 2. Unlike the instant claimed invention as per claim 6, Huang and Murugesh do not specifically disclose that the first power level is less than about 70 W.

However, Cheung discloses a method for depositing low dielectric constant film using PECVD comprises the step of using a low power level of 20-100 W (col 8, lines 10-12) overlaps the claimed range of less than 70W.

Hence, one skilled in the art would have found it obvious to modify Huang and Murugesh by using a low power level as per Cheung because Cheung states that silicon oxide/low k dielectric layers are most preferably produced using low level of RF power (col 3, lines 44-46)

5. Claims 9-10, 13-15, 18-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cheung et al (US 6,287,990) in view of Yew et al. (US 6,159,845) and further in view of Murugesh et al (US 6,228,781).

Cheung discloses a method for depositing a low k dielectric constant film at low power level. This method comprises the steps of:

depositing a layer of low k oxidized organosilane/ black diamond (see prior art of record for evidence of this basis) by plasma enhanced chemical vapor deposition (PECVD) using a gaseous mixture of dimethylsilane, nitrous oxide and helium at pulsed low level of RF power at 20 W to form a layer having a thickness (col 3, lines 29-48 and col 17, lines 1-6) reads on depositing a low power level of black diamond through PECVD from a gaseous mixture of methyl silane and nitrous oxide enhanced by a

plasma helium at a power level that is less than about 70 W to form a layer having a thickness

then depositing a dielectric layer having low dielectric constant such as FSG (fluorosilicate glass) using a gaseous mixture of dimethylsilane, nitrous oxide and helium at pulsed level of RF power at 150 W to form a layer having a thickness (col 8, lines 5-9 and col 14, lines 62-65) reads on depositing a high power layer of FSG by PECVD at a second power level that is higher than the first power level

patterning and etching the oxidized organosilane/black diamond layer to form a wiring trench (col 15, lines 6-9)

etching and patterning the wiring trench to the substrate/silicon wafer to form interconnect via/contact (col 15, lines 16-18 and fig. 8F)

depositing a copper layer to fill the via hole and trenches (col 15, lines 31-34 and fig. 8 H)

planarizing the structure using CMP leaving copper only inside the trench/via to form dual damascene structure that is free of cracking and peeling (col 15, lines 34-37 and fig. 8H shows a dual damascene structure that has no cracking or peeling)

Unlike the instant claimed invention as per claims 9 and 14, Cheung does not specifically disclose forming a higher power layer of black diamond although Cheung discloses forming a higher power layer of FSG.

However, Yew teaches forming inorganic dielectric material such as fluorosilicate glass (FSG) or black diamond using PECVD in a dual damascene interconnect structure (col 4, lines 1-4)

Hence, one skilled in the art would have found it obvious to modify Cheung by substituting the second layer of FSG with black diamond in view of Yew teaching because FSG and black diamond are known inorganic low dielectric material and the substitution of one for the other would have been anticipated to produce an expected result.

Cheung and Yew do not disclose repeating the steps of depositing the low dielectric constant material at low and higher power level for 10 seconds to reach a thickness of the low dielectric constant material layer

However, Murugesh discloses a method for depositing FSG (low k material) layer comprises the step of continuously depositing FSG layer at different power level (low and high) in a cycle (10-60 seconds) until the FSG layers reach a desired thickness (col 13, lines 36-38). Murugesh' s teaching reads on repeating the steps of depositing the low dielectric constant material at low and higher power level for 10 seconds to reach a thickness.

Hence, one skilled in the art would have found it obvious to modify Huang's method by adding the step of depositing the low dielectric constant material layer at low and higher power level until reaching a desired thickness as per Murugesh because Murugesh teaches that the cycle of deposition until FSG ayer having a desired thickness resulting in a film/layer having a low dielectric constant which has a good gap filling characteristic and stability (col 13, lines 38-40)

Regarding claims 10, 15, Cheung discloses depositing the FSG layer to a thickness of about 5000-10000 angstroms (col 15, lines 64-66)

Regarding claims 19-20, since Cheung discloses using reactive ion etching /plasma etching to pattern and etch the trench and the via hole and it is known in a method of plasma etching that etching variables such as temperature, time affect the amount of material removed by etching (see prior art of record for evidence of this basis). Thus, it would have been obvious to adjust the etching variable by conducting routine experimentations for the purpose of obtaining the specific depth and width of the trench or via hole.

Regarding claims 13 and 18, since it is known in the art that oxide /low dielectric constant material has a flat band voltage of –1.82 V exhibiting a low leakage current density (see prior art of record for evidence of this basis) , it would have been obvious to one skilled in the art to employ a low dielectric constant material having a flat band voltage that is less than about –3 V to achieve lower leakage current density

6. Claims 11-12, 16-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cheung et al (US 6,287,990) in view of Yew et al. (US 6,159,845) and further in view of Murugesh et al (US 6,228,781) and Puntamekar (US 5,821,603)

Cheung as modified by Yew and Murugesh have been described above in paragraph 5. Unlike the instant claimed inventions as per claims 11-12, 16-17, Cheung , Yew and Murugesh do not disclose the specific flow rate of the gases.

However, Puntambekar in a method for depositing dielectric layer using PECVD, discloses that gas flow rate can be varied to alter the resulting overall composition of the dielectric layer (col 4, lines 56-58)

Hence, one skilled in the art would have found it obvious to modify Cheung, Yew and Murugesh by vary/adjust the gas flow rate through routine experimentation in view of Puntambekar's teaching for the purpose of obtaining desired thickness/composition of the dielectric layer.

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Reber et al (US 6,159,559) discloses that oxide/dielectric layer has a flat band voltage of –1.82 V (col 7, lines 14-15)

Li et al (US 6,168,726) discloses that oxidized organosilane is a low k dielectric with a trade name of black diamond (col 3, lines 46-53)

Guinn et al (US 5,877,032) discloses that etching variables such as time, temperature can be varied to change the etch rate of photoresist or contact hole (col 4, lines 7-10)

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lan Vinh whose telephone number is 703 305-6302. The examiner can normally be reached on M-F 8:30-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Benjamin Utech can be reached on 703 308-3836. The fax phone numbers for the organization where this application or proceeding is assigned are 703 872-9310 for regular communications and 703 872-9311 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703 308-0661.

BENJAMIN L. UTECH
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 1700

LV
August 15, 2002